Synthesis and Characterizations of Ternary InGaAs Nanowires by a Two-Step Growth Method for High-Performance Electronic Devices

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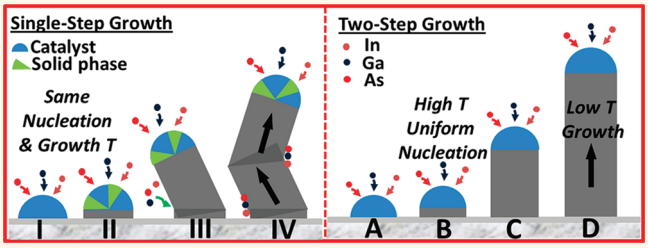
ABSTRACT



InAs nanowires have been extensively studied for high-speed and high-frequency electronics due to the low effective electron mass and corresponding high carrier mobility. However, further applications still suffer from the significant leakage current in InAs nanowire devices arising from the small electronic band gap. Here, we demonstrate the successful synthesis of ternary InGaAs nanowires in order to tackle this leakage issue utilizing the larger band gap material but at the same time not sacrificing the high electron mobility. In this work, we adapt a two-step growth method on amorphous SiO_2/Si substrates which significantly reduces the kinked morphology and surface coating along the nanowires. The grown nanowires exhibit excellent crystallinity and uniform stoichiometric composition along the entire length of the nanowires. More importantly, the electrical properties of those nanowires are found to be remarkably impressive with I_{ON}/I_{OFF} ratio $>10^5$, field-effect mobility of $\sim$2700 $cm^2/(V \cdot s)$, and ON current density of $\sim$0.9 mA/μm. These nanowires are then employed in the contact printing and achieve large-scale assembly of nanowire parallel arrays which further illustrate the potential for utilizing these high-performance nanowires on substrates for the fabrication of future integrated circuits.

KEYWORDS: indium gallium arsenide nanowires · two-step growth method · solid-source chemical vapor deposition · high-performance electronics · nanowire contact printing

In recent years, due to the low electron mass and corresponding high carrier mobility, indium arsenide (InAs) nanowires (NWs) has been extensively studied for high-speed and high-frequency electronic devices.[1−8] Meanwhile, because of the large Bohr radius, the InAs NW is also one of the excellent candidates to study quantum confinement effects.[9] However, further applications still suffer from the significant leakage current in InAs NW-based devices arising mainly from its small electronic band gap (0.34 eV). Although there has been significant progress in tackling this problem by altering the atomic structures, such as InAs/InP heterojunction[10] and InAsP segment along the InAs NWs,[11] a new NW materials system that does not rely on complicated heterostructures to solve the problem is still lacking.

Among many alternative materials, the ternary indium gallium arsenide (InGaAs) system is demonstrated as a promising thin-film channel material which has a relatively larger band gap to alleviate the leakage current issue and at the same time not sacrifice the high electron mobility;[12−14] nevertheless, there are few reports on the synthesis and characterization of this InGaAs NW material. Studies of terahertz emission[15] and photovoltaic[16] applications of InGaAs NWs have been recently demonstrated, but there is still very limited studies on the detailed fundamental electrical transport properties of InGaAs NWs. Importantly, those NWs are highly defective with significant twin defects and inversion domains,[15,17] which are expected to scatter carriers to degrade their electrical performance.[18−20] In this paper, we present a simple technique to synthesize highly crystalline InGaAs NWs by a novel two-step chemical vapor deposition (CVD) method with a high growth yield. From experimental results, the NWs exhibit impressive electrical performance with a I_{ON}/I_{OFF} ratio of $\sim 10^5$ and field-effect mobility of $\sim$2700 $cm^2/(V \cdot s)$ when configured in the back-gate NW field-effect transistors (FETs). Utilizing the NW printing approach,[21,22] high-performance InGaAs NW parallel array devices

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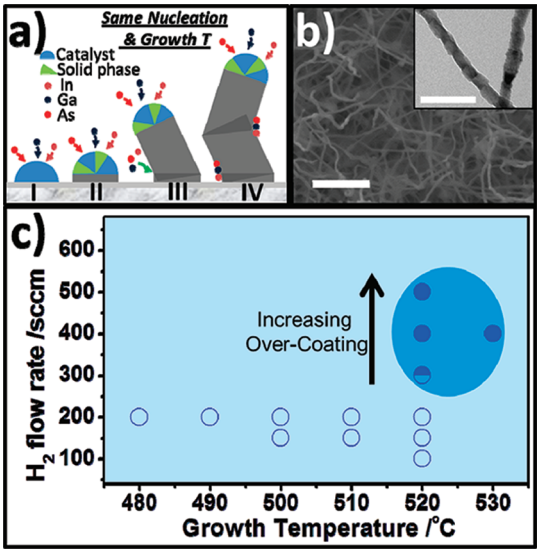

Figure 1. Single-step growth method. (a) Schematic of growth mechanism of the single-step method, demonstrating the kinked morphology and surface coating form gradually during the NW growth. (b) SEM and (inset) TEM images of NWs grown by the single-step method (growth condition: source temperature at 820 °C, substrate temperature at 520 °C, H_2 flow rate at 400 sccm, and growth duration for 30 min). The scale bars are 500 nm for SEM and 200 nm for TEM. (c) Growth process window summary of the single-step growth method, holding source temperature constant at 820 °C. Solid symbol designates the high NW growth density (>5 NW/μm^2), while open symbol indicates the low NW density (~1 NW/μm^2).

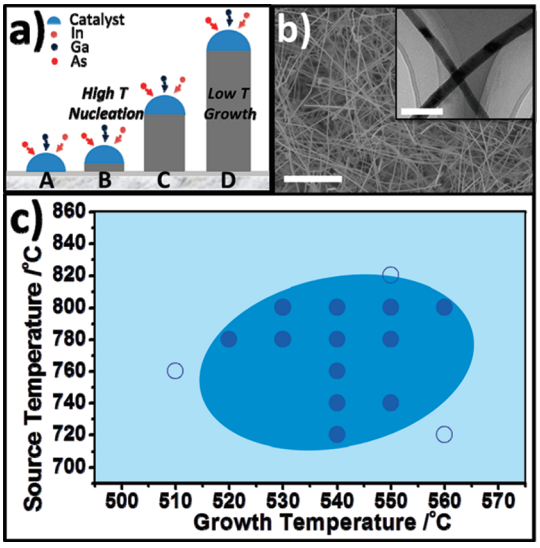

Figure 2. Two-step growth method. (a) Schematic of the growth mechanism of the two-step method. (b) SEM and (inset) TEM images of NWs grown by the two-step method (growth condition: source temperature at 800 °C, substrate temperature at 540 °C, H_2 flow rate at 100 sccm, growth duration of first step is 1 min and second step is 30 min); the scale bars are 2 μm and 200 nm, respectively. (c) Growth window summary of two-step method, holding H_2 flow rate at 100 sccm. Compared to single-step method, NWs produced by this two-step method have a much broader growth window, which provides the higher process parameter tolerance in the NW growth. Solid symbol designates the high NW growth density (>5 NW/μm^2), while open symbol indicates the low NW density (~1 NW/μm^2).

are fabricated, which further illustrates the technological potential of InGaAs NWs for next-generation electronic devices.

RESULTS AND DISCUSSION

InGaAs NWs used in this study were synthesized using a catalytic solid-source CVD method similar to the ones previously reported.[23,24] Here, only the In-rich InGaAs NWs would be the focus to ensure the opening of the band gap without degrading the excellent carrier mobility as compared to the ones of InAs NWs. Since the vapor pressure of Ga is higher than that of In atoms,[25,26] an equal weight of InAs and GaAs powders was mixed and utilized in this In-rich NW growth. In brief, during the growth, Au nanoparticles were used as catalysts and obtained by thermal annealing (~800 °C for 10 min) of a predeposited 0.5 nm thick evaporated Au layer on 50 nm thick SiO_2/Si substrates. Then the subsequent growth temperatures, both source and substrate zones, as well as flow rate of carrier gas, H_2, were carefully adjusted to control the physical properties of NWs. Notably, a two-step growth technique was adopted which has been utilized in other NW materials systems.[27,28] Compared to the conventional single-step CVD that contains only one regular growth step, the two-step approach has an additional nucleation step at a higher temperature before the regular growth step. Regarding our InGaAs NW system, this method could significantly reduce the kinked morphology, defect density, as well as surface coating around NWs compared to a single-step method.

Specifically, as shown in Figure 1a, in the single-step growth, Au catalysts were first formed on the substrate during the annealing stage. Afterward, the temperature was cooled to the growth temperature and the precursor vapors were started to supply from the source zone (stage I). However, at this moment, the catalyst nanoparticles may not be homogeneous in the liquid or solid phase because of similar temperatures between the catalytic eutectoids and the NW growth;[29] in this case, rather, some solid phase may coexist with the liquid phase within the catalysts (stage II), which is commonly observed in the synthesis of As-based NWs.[27,29] This physical phase inversion within the catalysts could hinder the growth rate of NWs at the catalyst−NW interface and lead to the unevenly distributed growth rate, which is the main reason of kinked morphology (stage III). Meanwhile, during the growth process, the precursor source atoms may impinge and diffuse onto the kinked surface due to the heterogeneous catalytic favorable sites.[30] When the growth time prolongs, all of these would eventually induce a severe overcoating problem (stage IV). As depicted in Figure 1b, InGaAs NWs grown by this single-step method have indeed serious kinked morphology. On the basis of the transmission electron

microscope (TEM) image (Figure 1b inset and see Supporting Information Figure S1), irregular surface coating exists along the entire length of the NWs. When the growth pressure or gas flow increases, the amount of coating gets more severe due to the shorter mean free path of precursor vapors. Importantly, after summarizing the results of more than 50 growth trails, the process window of this single-step approach is found to be quite narrow, as illustrated in Figure 1c; only growth temperatures of 520−530 °C and H_2 gas flow higher than 300 sccm (source temperature constant at 820 °C) can produce NWs with a decent density (>5 NW/μm^2). Any other conditions deviated from this window would not result in any NW growth or gives NWs with a very low growth yield (<1 NW/μm^2). This tight window would be mainly attributed to the inhomogeneous catalytic phase which makes the NW nucleation process difficult and sensitive to the growth temperature and pressure.

In contrast, as demonstrated in Figure 2b and its inset, InGaAs NWs grown by the two-step method exhibit much more straightness as well as smoother surface (no overcoating). These obvious differences could be explained by the difference in growth mechanisms between these two techniques. In the two-step growth approach, the first nucleation step is performed at a higher temperature (~600 °C), significantly reducing the chances of solid phase formation within the catalysts (stages A and B). Therefore, NWs will grow more uniformly at the catalyst−NW interface and nurture along a certain growth direction without the kinked structures formed; this way, the source vapor atoms would not easily deposit onto the NW surface directly to form the surface coating, and they will be more likely to migrate into the catalyst region following the standard vapor−liquid−solid (VLS) growth process (stages C and D). The two-step grown InGaAs NWs are typically found to have a length exceeding 10 μm and an average diameter of 30 nm uniformly along the length of the NWs. In this case, this two-step method is expected to be less sensitive to the growth condition. As shown in Figure 2c, summarizing more than 100 growth trials, there is indeed a much wider growth process window spanning the source and growth temperatures between 720−800 and 520−560 °C, respectively, and a low gas flow of H_2 (~100 sccm) is purposely utilized to minimize the formation of overcoating. Notably, this broad experimental parameter tolerance will certainly offer a great processing flexibility for the synthesis of InGaAs and other III−V NWs.

In order to further characterize the NWs grown by this two-step technique, high-resolution TEM (HRTEM) is utilized to study the structural properties of these NWs. As depicted in Figure 3a, a spherical catalytic seed is observed at the tip of a typical NW, which confirms the VLS growth mechanism. The corresponding selected area electron diffraction (SAED) pattern further illustrates its single-crystalline zinc blende (ZB) structure and its preferential growth orientation in the ⟨111⟩ direction (see Supporting Information Figure S2). This growth direction is dominant in other observed NWs, which corresponds well to several studies in III−V nanowire synthesis where the ⟨111⟩ direction is the major one because of the lowest surface energy in {111} planes.[31,32] Although there are a few dark bands in the low-resolution TEM image (Figure 2b), which are believed to be stacking faults, however, the majority of the NWs are uniform and in the low defect concentration, as demonstrated in the HRTEM image in Figure 3b. Also, the spacings between the adjacent lattice planes are found to be 0.34 and 0.29 nm, which are in good agreement with the plane spacing of {111} and {200} equivalent planes in the In-rich thin-film counterparts, respectively.[33] The thickness of the native oxide amorphous layer is about 2.5 nm, which is consistent with other reported III−V 1D nanostructures.[2,25] Notably, no wurtzite structure is observed under SAED or HRTEM characterization. All of these indicate the good crystallinity of NWs grown by this two-step technique.

Moreover, one of the challenges in synthesizing high-performance III−V nanowires is to control the NW stoichiometry uniformly and precisely to enable various devices fabrications. For ternary NWs such as InGaAs, this stoichiometric problem appears to be even more challenging because the chemically increased degree of freedom may easily induce atomic aggregation and clusters in the NW body, degrading the electrical properties of NWs.[18−20] In this case, as shown in Figure 3c, the energy-dispersive X-ray spectrometric (EDS) elemental mapping of same NW (Figure 3a,b) demonstrates the homogeneous distribution of In, Ga, and As atoms along the NW body. To further shed light to quantify the corresponding chemical composition, EDS line scan is performed along the NW axial direction across from the tip to body (see Supporting Information Figures S3 and S4). On the basis of the line scan, the catalyst mainly contains In and Au atoms while the Au content drops drastically once passing the catalyst-NW interface. This observation suggests that no significant Au diffusion occurs in NW body which may damage the crystallinity and electrical properties, and the approximate AuIn composition in the catalyst agrees well with the previous report on Au-catalyzed InAs NWs.[34] Also, no As concentration is found in the tip, indicating that the solubility of As in Au eutectoids is low[35] and As atoms would react in the tip/NW interface to induce the NW growth.[34−36] On the other hand, little Ga content exists in the catalyst, which could be attributed to the faster diffusion of Ga compared to In atoms and also the purposely Ga deficient precursor vapors; therefore, Ga atoms are continuously consumed in the growth interface for the formation of In-rich NWs. In addition, more than 10 NWs are studied by the EDS analysis in detail, and they all exhibit the NW composition of $In_xGa_{1-x}As$ with x ranging from 0.65 to 0.73. All of these have demonstrated the remarkably

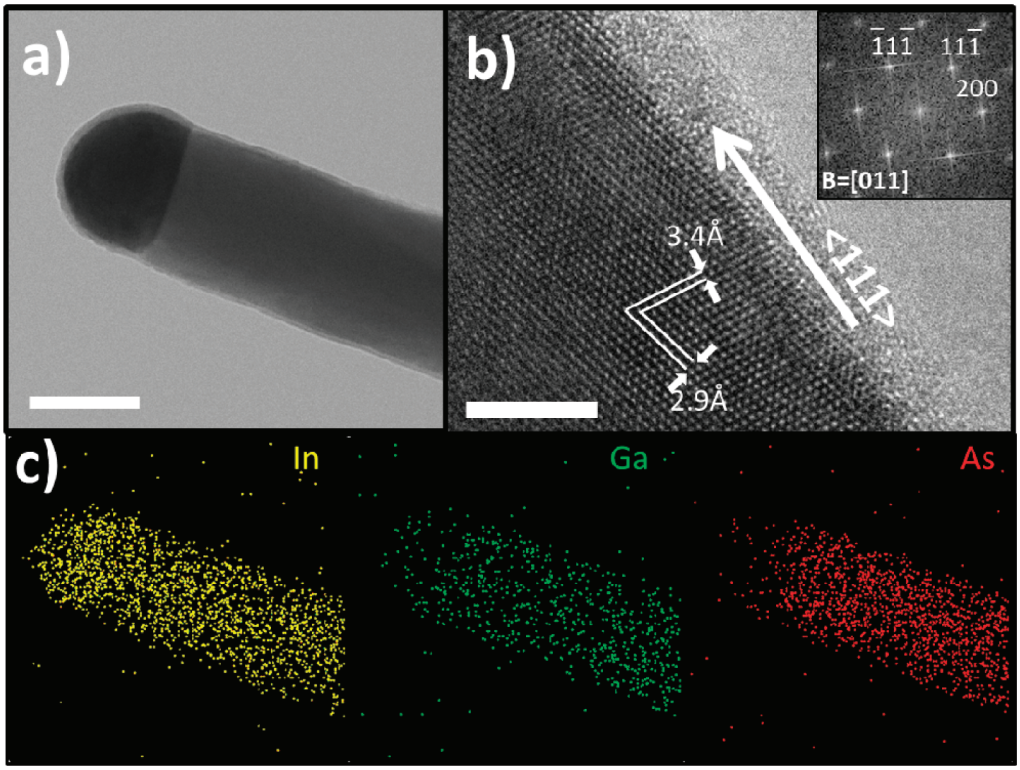

Figure 3. Typical single-crystalline NW with the uniform stoichiometry. (a) STEM image of a representative InGaAs NW. (b) HRTEM of the corresponding NW. The scale bar is 5 nm. (Inset) Fast Fourier transform (FFT) image of the NW body, showing a ZB structure with the ⟨111⟩ growth direction; (c) EDS elemental mapping of the NW in panel a. The representative NW has uniform In-rich composition across the NW body.

good control of the NW stoichiometry with this simple two-step technique. Notably, it would be fundamentally interesting to vary the NW composition to Ga-rich regions and study their corresponding physical properties; however, a recent study of $In_{0.5}Ga_{0.5}As$ and other Ga-rich NWs showed the high defect density[15] probably deteriorating the carrier transport along the NW,[18−20] while more investigation is currently in process.

To shed light studying the electrical properties of InGaAs NWs, as shown in Figure 4a, field-effect transistors (FETs) were fabricated by using Ni (∼50 nm) source/drain (S/D) metal contacts in a common back-gated configuration (50 nm thermal oxide as the gate dielectric and heavily B-doped Si substrate as the gate). The electrical performance of a representative FET consisting of an individual InGaAs NW as the channel material with the diameter of $d \sim 21$ nm (NW diameter ∼ 26 nm with ∼5 nm native oxide shell) and a channel length of $L \sim 2.64$ μm is shown in Figure 4b. The NW FET exhibits n-type conduction as expected, and under $V_{DS} = 1$ V, it achieves 19 μA ON current under $V_{GS} = 5$ V and a 100 pA OFF current under $V_{GS} = -7$ V. This ON current corresponds to a current density of ∼0.9 mA/μm as normalized with the NW diameter (effective channel width), which is comparable to that of the state-of-the-art Si MOSFETs (∼1 mA/μm). Although this ON current is similar to the InAs NW FET,[3] consequently, it gives a much better I_{ON}/I_{OFF} ratio (∼10^5; see Supporting Information Figure S5). In contrast to another previous study of InGaAs NWs grown by MOVPE, the same I_{ON}/I_{OFF} ratio can only be obtained for the measurement performed at 1.5 K.[37] Also, the ON−OFF ratio statistics (Figure 4b inset) further demonstrate this typically high ratio (>10^4) being dominant across all of the devices, as ∼80% of 100 measured devices fall into this category. Furthermore, the corresponding field-effect mobility is calculated in Figure 4c as a function of back-gate voltage V_{GS}. Specifically, the transconductance ($g_m = (dI_{DS})/(dV_{GS})|V_{DS}$) at low bias $V_{DS} = 0.1$ V is assessed, and the mobility is deduced by standard square law model $\mu = g_m(L^2/C_{ox})(1/V_{DS})$, where C_{ox} is the gate capacitance obtained from the finite element analysis software COMSOL with respect to the different diameter of the nanowire. The calculated peak mobility is about ∼2700 $cm^2/(V \cdot s)$, which is comparable to the state-of-the-art InAs NW FET.[2] All of these have indicated the excellent crystal quality of NWs achieved in this simple two-step technique.

In order to further demonstrate the feasibility of large-scale integration of the NWs for electronic applications, the well-established NW contact printing method[1,23,24] is utilized to fabricate InGaAs NW parallel arrays following the same device fabrication. Figure 5a shows the SEM image and schematic of the printed NW array FET, while Figure 5b demonstrates the electrical transport of a printed array with ∼200 nanowires in the channel (width ∼200 μm and length ∼2 μm).

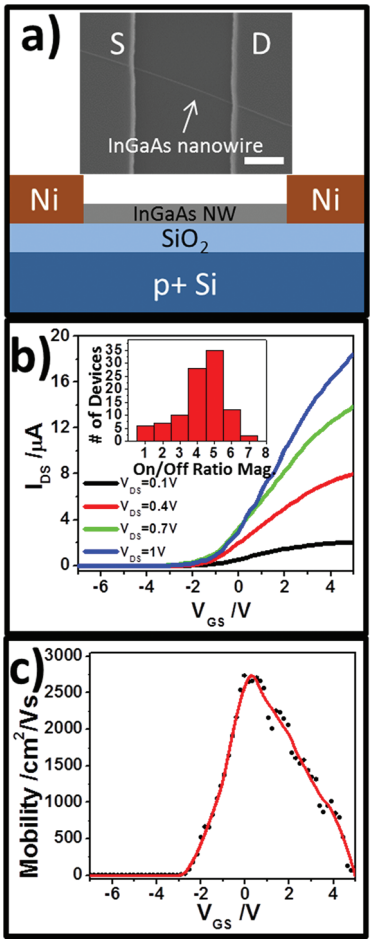

Figure 4. Electrical characterization of the representative single NW FET. (a) (Top) SEM image and (bottom) schematic of a back-gated InGaAs nanowire FET with Ni S/D metal contacts; the scale bar is 1 μm. (b) Transfer characteristic of a back-gated InGaAs NW FET with $d \sim 21$ nm and $L \sim 2.6$ μm for $V_{DS} = 0.1$, 0.4, 0.7, and 1 V. The inset shows the statistics of I_{ON}/I_{OFF} ratio sampling from 100 InGaAs NW FET devices obtained from the same NW growth trial. (c) Mobility assessment under $V_{DS} = 0.1$ V of the device in panel b. The black dotted line is the experiment data, and the solid red line is the fitted data curve.

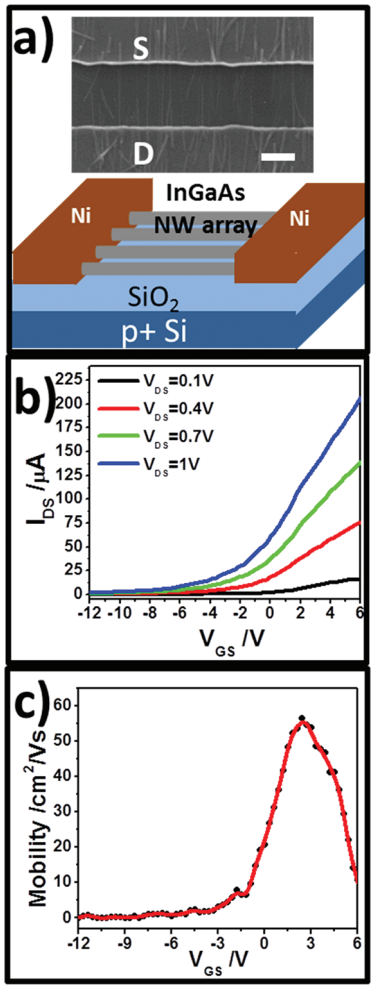

Figure 5. Electrical characterization of the representative InGaAs NW parallel array FET. (a) (Top) SEM and (bottom) schematic of a back-gated InGaAs NW array FET. The scale bar is 1 μm. The designated channel length and width are 2 and 200 μm, respectively. (b) Transfer characteristic of a representative InGaAs NW parallel device under $V_{DS} = 0.1$, 0.4, 0.7, and 1 V, about 200 NWs bridging S/D. (c) Mobility assessment of this NW array device under $V_{DS} = 0.1$ V. The black dotted line is the experimental data, and the solid red line is the fitted data curve.

This device delivers a current density of 1 μA/μm under $V_{DS} = 1$ V and $V_{GS} = 6$ V, with an I_{ON}/I_{OFF} ratio of ~500 (see Support Information Figure S6). As shown in Figure 5c, the corresponding field-effect mobility against gate voltage V_{GS} is also evaluated, and the mobility is calculated based on the standard square law model similar to the operation of the single NW device. The capacitance is estimated using an upper-bound model that multiplies the capacitance from every single nanowire and the number of nanowires in the channel.[38] The calculated peak mobility is found to be ~60 $cm^2/(V \cdot s)$ and on the same level of the state-of-the-art semiconductor carbon nanotube networks.[39] Compared to the single NW device (Figure 4), the average current level of each NW gets degraded, which could be attributed to different NW-to-NW gate coupling due to the misalignment and broken wires in the channel leading to the parasitic capacitance, both of which will significantly increase the total capacitance and decrease current output. Further enhancement of the mobility can be achieved in the future by the passivation of the NW surfaces such as the $(NH_4)_2S$ treatment,[40−42] while current investigations are ongoing. In the future, the NW device performance can also be further improved through the enhancement of NW print density, alignment, channel length scaling, and the integration of high-k dielectric in the top-gated structures.

CONCLUSION

In conclusion, a two-step growth method in the solid-source chemical vapor deposition to synthesize ternary InGaAs nanowires is presented. This approach could significantly reduce the kinked morphology and issue of surface coating problem. The grown InGaAs

nanowires have remarkable single crystallinity as well as uniformly distributed stoichiometric composition of In, Ga, and As based on this simple growth technique. By fabricating back-gate field-effect transistors, the impressive ON current densities (~0.9 mA/μm, I_{ON}/I_{OFF} ratio (>10^5), and electron mobility (~2700 $cm^2/(V \cdot s)$) are obtained, demonstrating the success of lowering the leakage current without sacrificing the carrier mobility as compared to the state-of-the-art InAs nanowire devices. These InGaAs nanowires are then employed in the contact printing and generate large-scale assembly of nanowire parallel arrays that could be utilized in the fabrication of future high-performance integrated circuits.

METHODS

Nanowire Synthesis. InGaAs nanowires were synthesized on an amorphous SiO_2/Si wafer in a two-zone furnace using a chemical vapor transport method. InAs and GaAs powders were mixed in a designated ratio (50 wt % InAs/50 wt % GaAs) and loaded into a boron nitride crucible in the upstream of the furnace. The growth substrate, deposited with 0.5 nm Au film in thermal evaporator, was positioned in the downstream. H_2 (99.9995%) was used as carrier gas to transport the evaporated source materials to the growth substrate. The temperature in the downstream was first elevated to 800 °C and remained at that temperature for 10 min in order to anneal the Au catalyst. For the single-step growth method, the temperature was then cooled directly to the growth temperature (~15 min after annealing stop). Then the upstream started to heat, and when the source temperature reached the designated value, the growth began. For the two-step growth method, the substrate temperature was first cooled to the nucleation temperature (~10 min after annealing) when the source temperature started to elevate. When the source temperature reached the designated value, the nucleation step began. After 1−2 min, the downstream stopped heating and started to cool again to a second step growth temperature (approximately 6−8 min after heating stop). During the growth, the flow rate of H_2 was maintained at 100 sccm and the corresponding pressure downstream is ~1 Torr. The grown nanowires were taken out of the furnace after the system was cooled naturally to room temperature.

Single NW Device Fabrication and Characterization. After CVD growth, the InGaAs nanowires were first harvested by sonication in high-purity ethanol solution. Then we randomly drop-cast the nanowires onto precleaned highly doped p-type Si substrates, with a 50 nm thermal grown gate oxide. These substrates, 1.5 cm × 1.5 cm in size, were then spin-coated with LOR and AZ5206 photoresist and were exposed to ultraviolet light and went through developing. After we get the source and drain pattern, a 50 nm thick Ni will be thermally deposited as the contact electrodes followed by a lift-off process. Electrical performance of fabricated back-gated FETs was characterized with a standard electrical probe station and Agilent 4155C semiconductor analyzer.

Printing Device Fabrication and Characterization. NW arrays were printed on doped p-type SiO_2/Si substrates, and these substrate were then spin-coated with LOR and AZ5206 photoresist and went through lithography and developing, followed by Ni electrode deposition and lift-off. Before electrical characterization, the NW arrays were then soaked in $(NH_4)_2S$ solution in order to passivate the surface of the NWs. After passivation, the devices were rinsed carefully using DI water and ethanol and baked at 120 °C for 60 min. Electrical performance of fabricated NW array FETs was then characterized with a standard electrical probe station and Agilent 4155C semiconductor analyzer.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: TEM images of the kinked NW with surface coating; SAED of a typical InGaAs NW; the corresponding EDS line scan on the NW; EDS spectrum within the NW body; electrical I−V measurements of the single NW FET and parallel nanowire array FET, respectively. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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